iU6392A

3-Phase BLDC Motor Controller

Datasheet Rev. 0.5

1. Description

The iU6392A is a 3-phase BLDC motor controller IC integrated with various peripherals to realize sensor or sensor-less BLDC motors application, including FOC. The logic input is compatible with standard CMOS output. It features the flexibility to adjust various motor parameters and complete protection such as over current, over voltage and under voltage lockout.

2. Features

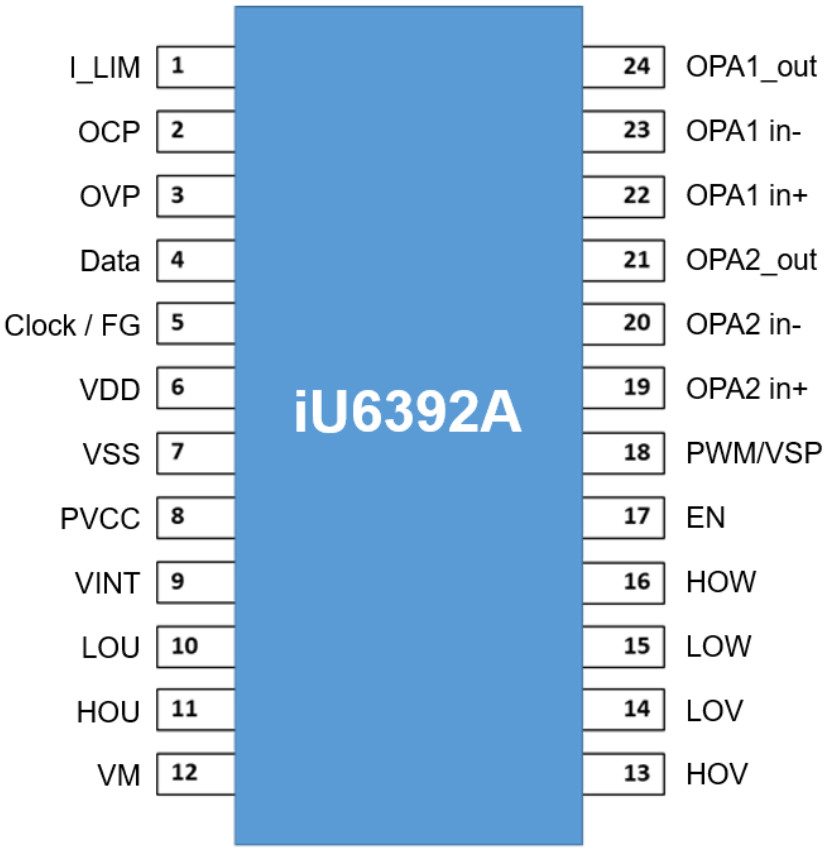
- Three-Phase BLDC Motor Controller
- Operating Supply Voltage from 7V to 32V
- Integrated Current Amplifier x 2
- Embedded P/N MOS Pre-driver
- Programmable Locked Rotor and Restart Timing
- Programmable Soft Start Timing
- Complete Protection OCP/OVP/UVLO
- TSSOP-24 Package

3. Applications

- BLDC Motor Driver

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4. Pin Assignments



5. Marking Information

Product Name	Marking
iU6392A	 X: Date code

6. Ordering Code

Ordering Code
iU6392A

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7. Pin Definitions

Pin No.	Symbol	Description
1	I_LIM	Average Current Detection
2	OCP	Over Current Protection
3	OVP	Over Voltage Protection
4	Data	Data Input
5	Clock / FG	Clock Input / FG
6	VDD	Self Logic 5V Power
7	VSS	Ground
8	PVCC	Power VCC Supply
9	VINT	7V Regulator Output for Pre-Driver
10	LOU	U-Phase, Low Side Gate Driver
11	HOU	U-Phase, High Side Gate Driver
12	VM	VDC Supply, HO Pull-Hi Voltage
13	HOV	V-Phase, High Side Gate Driver
14	LOV	V-Phase, Low Side Gate Driver
15	LOW	W-Phase, Low Side Gate Driver
16	HOW	W-Phase, High Side Gate Driver
17	EN	Pre-Driver Enable
18	PWM/VSP	PWM/VSP
19	OPA2 in+	OPAMP2 Positive Input
20	OPA2 in-	OPAMP2 Negative Input
21	OPA2_out	OPAMP2 Output
22	OPA1 in+	OPAMP1 Positive Input
23	OPA1 in-	OPAMP1 Negative Input
24	OPA1_out	OPAM1 Output

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8. Electrical Characteristics

8.1 Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Parameter	Min.	Max.	Unit
V_{HO}	High Side Floating Output Voltage	VM - 7	VM + 0.3	V
PVCC	Low Side Power Supply Voltage	- 0.3	40	V
VM	High Side Power Supply Voltage	- 0.3	40	V
I/O Pin	Logic Input Voltage	- 0.3	VDD + 0.3	V
T_J	Junction Temperature	-	125	℃
T_S	Storage Temperature	-55	150	

8.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
PVCC	Low Side Power Supply Voltage	7	32	V
I/O Pin	Logic Input Voltage	0	VDD + 0.3	V
T_A	Ambient Temperature (*Note)	- 40	105	℃

*Note：Please do not exceed Tj limitation

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8.3 D.C. Characteristics

Symbol	Conditions			Min.	Typ.	Max	Unit
	Mode	f_{HCLK}	Conditions				
IDD	Operation Mode Internal Clock	60MHz	All Peripherals Enabled	-	8.61	-	mA
			All Peripherals Disabled	-	7.08	-	mA
		40KHz	All Peripherals Enabled	-	1.02	-	mA
			All Peripherals Disabled	-	1.00	-	mA
	Sleep Mode, Internal Clock	60MHz	All Peripherals Enabled	-	3.52	-	mA
			All Peripherals Disabled	-	2.25	-	mA
		40KHz	All Peripherals Enabled	-	1.00	-	mA
			All Peripherals Disabled	-	1.00	-	mA
	Stop Mode	-	Enter Stop Mode after Reset	-	110	-	uA

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8.4 A.C. Characteristics

8.4.1 High Speed Internal Oscillator (HSI) Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
f_{HSI}	Frequency	-	-	60	-	MHz
ACC_{HSI}	Accuracy of HSI Oscillator	T_A = -40°C ~ 105°C	-2.5	-	+2.5	%
		T_A = -10°C ~ 85°C	-1.5	-	+1.5	%
		T_A = 25°C	-1	-	+1	%

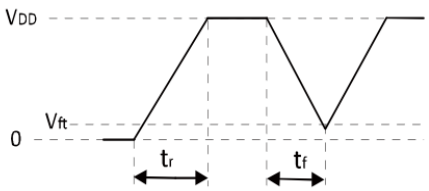
8.4.2 Low Speed Internal Oscillator (LSI) Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
F_{LSI}	Frequency	T_A = -40°C ~ 105°C	20	40	60	KHz
$tsu_{(LSI)}$	LSI Oscillator Start-up Time	-	-	-	300	us
$IDD_{(LSI)}$	Power Consumption of LSI Oscillator	-	-	0.34	-	uA

8.4.3 Power-up and Power-down Characteristics

Symbol	Conditions	Min.	Typ.	Max	Unit
t_{VDD}	VDD Rising Time tr	300	-	50000	us
	VDD Falling Time tf	300	-	50000	
V_{ft}	Power-down Threshold Voltage	0	-	-	mV

Note 1：Derived from overall evaluation, not tested in production.
Note 2：The on-chip VDD waveform during power-down should follow the tr and tf stages as shown in the waveform diagram below.
Note 3：The chip should be powered up from 0V to ensure reliable power-up.



8.4.4 Low-Power Mode Wake-up Time

Symbol	Conditions	Min.	Typ.	Max	Unit
$t_{WUSLEEP}$	Wake-up from Sleep Mode (System Clock is HSI)	-	1.5	-	us
t_{WUSTOP}	Wake-up from Stop Mode (System Clock is HSI)	-	65	-	us

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8.5 Input / Output Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
V_{IL}	Input low-level voltage	5V CMOS port	-	-	0.3 * VDD	V
V_{IH}	Input high-level voltage	5V CMOS port	0.7 * VDD	-	-	V
V_{hy}	I/O pin Schmitt trigger voltage hysteresis	5V	0.1 * VDD	0.60	-	V
I_{lkg}	Input leakage current	5V	-1	-	1	μA
R_{PU}	Weak pull-up equivalent resistor	5V VIN = VSS	50	60	75	kΩ
R_{PD}	Weak pull-down equivalent resistor	5V VIN = VSS	50	60	75	kΩ
C_{IO}	I/O pin capacitance	-	-	-	10	pF

Symbol	Parameter	Conditions	Typ.	Unit
V_{OL}	Output low level	$\|I_{IO}\|$ = 6mA，VDD = 5V	0.11	V
V_{OH}	Output high level		4.83	
V_{OL}	Output low level	$\|I_{IO}\|$ = 8mA，VDD = 5V	0.15	
V_{OH}	Output high level		4.78	
V_{OL}	Output low level	$\|I_{IO}\|$ = 20mA，VDD = 5V	0.38	
V_{OH}	Output high level		4.4	

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8.6 POR / PVD Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
V_{PVD}	Level Selection for Programmable Voltage Detector	Rising Edge: Level 1	-	2.4	-	V
		Falling Edge: Level 1	-	2.3	-	V
		Rising Edge: Level 2	-	2.7	-	V
		Falling Edge: Level 2	-	2.6	-	V
		Rising Edge: Level 3	-	3.0	-	V
		Falling Edge: Level 3	-	2.9	-	V
		Rising Edge: Level 4	-	3.3	-	V
		Falling Edge: Level 4	-	3.2	-	V
		Rising Edge: Level 5	-	3.6	-	V
		Falling Edge: Level 5	-	3.5	-	V
		Rising Edge: Level 6	-	3.9	-	V
		Falling Edge: Level 6	-	3.8	-	V
		Rising Edge: Level 7	-	4.2	-	V
		Falling Edge: Level 7	-	4.1	-	V
		Rising Edge: Level 8	-	4.5	-	V
		Falling Edge: Level 8	-	4.4	-	V
		Rising Edge: Level 9	-	4.8	-	V
		Falling Edge: Level 9	-	4.7	-	V
V_{POR}	Power-on Reset Threshold	-	-	2.2	-	V
$V_{hyst_POR/PDR}$	POR/PDR Hysteresis	-	-	60	-	mV
$T_{RSTTEMPO}$	Reset Duration	-	-	1.84	-	ms

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8.7 A/D Converter Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
V_{DD}	Supply Voltage	-	2.5	-	5.5	V
f_{ADC}	ADC Clock Frequency	VDD ≥ 2.5V	-	-	15	MHz
f_S	Sampling Rate	12bits; VDD ≥ 2.5V	-	-	1	MHz
f_{TRIG}	External trigger frequency	12bits; f_{ADC} = 15MHz	-	-	1	MHz
		12bits	-	-	15	1/ fADC
R_{AIN}	External Input Impedance	-	See the formula below			KΩ
R_{ADC}	Sampling switch resistance	-	-	-	1.5	KΩ
C_{ADC}	Internal sampling and holding capacitance	-	-	-	5	pF
t_{STAB}	Power-up Time	-	-	-	10	μS
t_{lat}	Injection-Trigger Conversion Delay	-	-	-	512	1/fADC
t_{latr}	Regular-Trigger Conversion Delay	-	-	-	512	1/fADC
ts	Sampling Time	f_{ADC} = 15MHz	0.167	-	16.03	μS
t_{CONV}	Total Conversion Time (including Sampling Time)	12bits; f_{ADC}=15MHz	1	-	16.87	μS
ENOB	Effective Number of Bits	12bits; VDD ≥ 3.3V; f_{ADC} = 15MHz	-	10.9	-	bit

Note: For external triggering, a delay of 1/f_{ADC} must be added to the timing

Input Impedance Table

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times ln(2^{n+2})} - R_{ADC}$$

The above formula is used to determine the maximum external impedance to ensure that the error is less than 1/4 LSB. Here, n = 12 (representing 12-bit resolution) and it is measured at f_{ADC} = 15MHz.

Symbol	Parameter	Conditions	Typ.	Unit
ET	Overall Error	f_{PCLK1}=60MHz, f_{ADC}=15MHz, R_{AIN}<0.1KΩ, VDD=5V, T_A=25°C	-4.7 to +3.4	LSB
EO	Offset Error		-1.9 to +2.8	LSB
EG	Gain Error		-0.4 to +1.6	LSB
ED	Differential Linearity Error		-1.0 to +0.4	LSB
EL	Integral Linearity Error		-2.2 to +3.4	LSB

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8.8 Operational Amplifier Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
V_{DD}	Supply Voltage	-	2.5	-	5.5	V
V_{OFFSET}	Input Bias Voltage	-	-	1	-	mV
I_{LOAD}	Drive Current	Drive current (sinking current) (VDD=5V, VOUT=1V)	-	-	15	mA
C_{LOAD}	Capacitive Load	-	-	-	30	pF
CMRR	Common Mode Rejection Ratio	-	-	80	-	dB
PSRR	Power Supply Rejection Ratio	-	-	80	-	dB
GBW	Gain-Bandwidth Product	-	-	12	-	MHz
SR	Slew Rate	-	-	7	-	V/us
GOL	Open-loop Gain	-	90	110	120	dB

8.9 Comparator Electrical Characteristics

Symbol	Parameter	Register Configuration	Min.	Typ.	Max	Unit
t_{HYST}	Hysteresis	00(hysteresis), high power	-	0	-	mV
		00(hysteresis), low power	-	0	-	mV
		01(hysteresis), high power	15	22	43	mV
		01(hysteresis), low power	13	15	23	mV
		10(hysteresis), high power	32	45	92	mV
		10(hysteresis), low power	25.2	32	46.7	mV
		11(hysteresis), high power	55	85	182	mV
		11(hysteresis), low power	25.5	60	83.9	mV
V_{OFFSET}	Offset Voltage	-		+/-6	+/-10.4	mV
t_{DELAY}	Propagation Delay Note1	00（high power）	3.7	10.7	43	ns
		01（medium power）	10.5	34.9	83	ns
		10（low power）	13.8	49	114	ns
		11（ultra-low power）	22.2	86	194.5	ns
Iq	Average Operating Current	00（high power）	6.5	45	205.4	μA
		01（medium power）	3.3	21.7	81.3	μA
		10（low power）	2.6	15.3	59.6	μA
		11（ultra-low power）	1.7	8.8	35.3	μA

Note1 : Time difference between 50% output transistor and input transition.

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8.10 P/N MOSFET Gate-driver with LDO Electrical Characteristics

8.10.1 Driver Section

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
V_{HSOH}	Hi-side PMOS off, VM - VHO	I_O = 2mA	-	0.24	-	V
V_{LSOH}	Low-side NMOS off	I_O = 2mA	-	VINT - 0.2	-	V
I_{HOL}	High-Side turn-on current	-	-	35	-	mA
I_{LOH}	Low-Side turn-on current	-	-	45	-	mA
Iop	Operating current	-	-	-	30	mA
V_{CCUV+}	PVCC supply under voltage positive going threshold	-	6.2	6.6	7	V
V_{CCUV-}	PVCC supply under voltage negative going threshold	-	5.9	6.3	6.7	V
V_{HOCLP}	HO clamp, VM - VHO	-	6.5	7	7.5	V

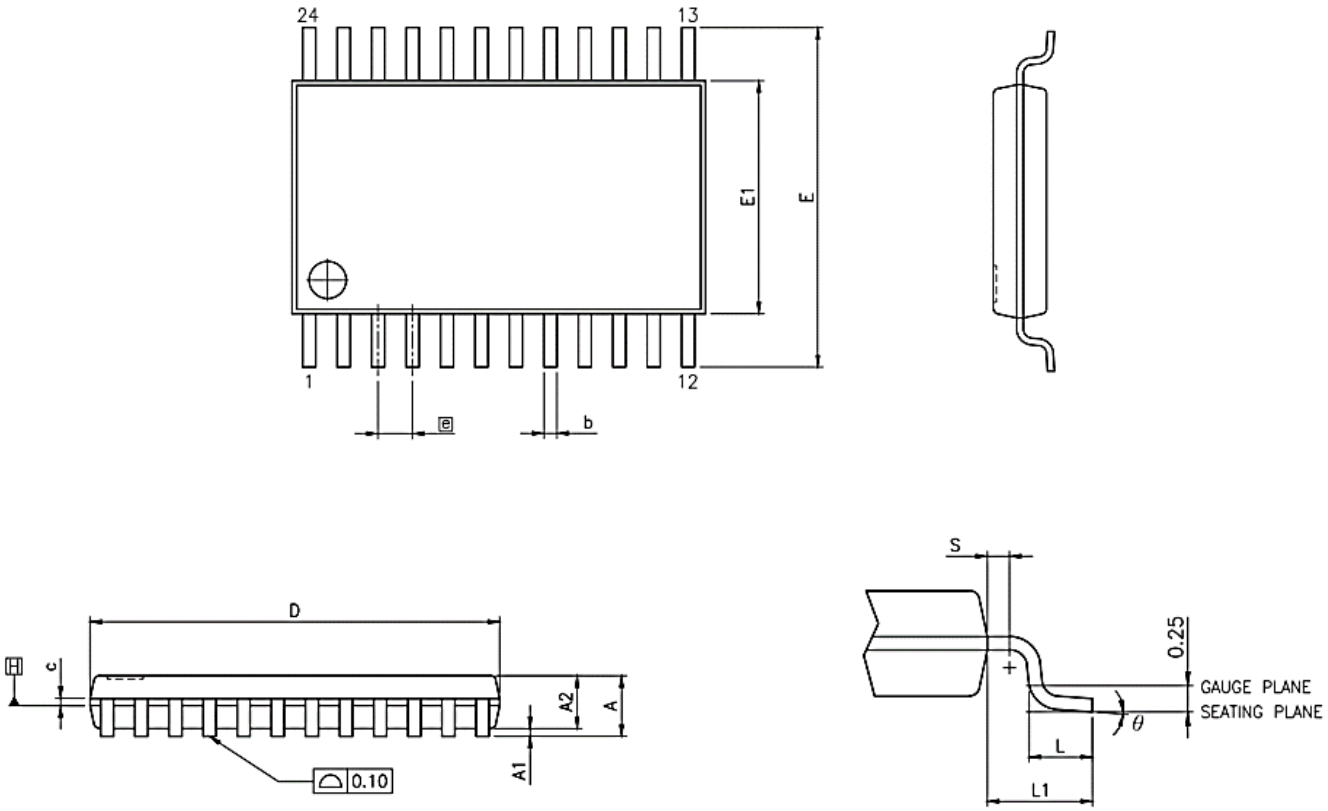
8.10.2 LDO Section

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
V_{INT}	Internal regulator output voltage	I_{VINT} = 5 mA	6.5	7	7.5	V
I_{VINT}	VINT output current	VINT = 6.5 V	10	-	-	mA
VDD	5V regulator output voltage	I_{VDD} = 10 mA	- 5%	5	+ 5%	V
IV_{DDMAX}	VDD max output current	VDD = 4.5 V	-	-	20	mA

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9. Package Information

TSSOP-24 Outline Dimensions



SYMBOL	Dimension in mm		
	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	7.70	7.80	7.90
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	-	-
θ	0°	–	8°

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